REMARKS

Claims 1-3, 15 and 18 have been amended to improve form and claims 16 and 17 have been canceled without prejudice or disclaimer. Claims 1-15 and 18-20 are now pending in this application.

The applicants acknowledge, with appreciation, the indication that claims 7-14 have been allowed and claims 18-20 have been indicated as allowable if rewritten in independent form.

Claims 1-6 and 15-17 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Aydemir et al. (U.S. Patent No. 6,771,601; hereinafter Aydemir). The rejection is respectfully traversed.

Initially, the applicants note that the grounds of rejection under 35 U.S.C. § 102(e) based on Aydemir includes claims 1-6 and 15-17 (Office Action – page 2). Claim 6, however, has been rejected under 35 U.S.C. § 103 based on the combination of Aydemir and Rom et al. (Office Action – page 8). Therefore, the applicants assume that claim 6 was inadvertently included in the grounds of rejection under 35 U.S.C. § 102(e) based on Aydemir since claim 6 was not particularly addressed in the rejection under 35 U.S.C. § 102(e). Claim 6 will therefore be addressed below with respect to the rejection under 35 U.S.C. § 103. If this is not the case, clarification as to the grounds of rejection is respectfully requested in any subsequent communication.

Claim 1 recites a method that includes receiving a data frame on a first logic component of a network device, identifying receive port information associated with the data frame, the receive port information identifying a port on the first logic component on which the data frame was received, and transmitting the data frame and the receive port information to a second logic component on the network device, based on a destination address of the data frame. Claim 1 also

recites receiving the data frame and receive port information at the second logic component and storing the receive port information on the second logic component.

The Office Action states that Aydemir disclose transmitting a data frame to a second logic component (Fig. 2, device 10') based on a destination address of the data frame and receiving the data frame at the second logic component and points to col. 7, lines 6-17 of Aydemir for support (Office Action – page 3). The applicants note that the Office Action does not allege that Aydemir discloses that component 10' receives or stores receive port information associated with the data frame, as required by claim 1. The applicants respectfully request that any subsequent communication point out where Aydemir allegedly discloses this feature or withdraw the rejection.

In any event, Aydemir at col. 7, lines 6-17 discloses that switch 10 stores data from input ports 12a-12z in output port sub-queues 18a-18z and forwards the data via output port 14a to switch 10'. Switch 10' then queues the received data in its own output port sub-queues 18a'-18z'. Aydemir does not disclose or suggest that switch 10 transmits the receive port information to switch 10' or that switch 10' stores any receive port information, as required by claim 1.

Claim 1, as amended, also recites generating a pause frame by the first logic component in response to receiving the receive port information from the second logic component, and transmitting the pause frame by the first logic component via the port identified by the receive port information. A similar feature was previously recited in original claim 3.

With respect to original claim 3, the Office Action states that Aydemir discloses transmitting a pause frame via the port identified by the receive port information and points to col. 8, lines 53-65 for support (Office Action – page 4). The applicants respectfully disagree.

Aydemir discloses that if switch 10' detects congestion associated with an output queue as a result of data transmitted over link 30, switch 10' transmits a pause message to switch 10, where the

pause message includes a message identifier associated with the data which resulted in the detection of the congestion condition (Aydemir – col. 7, lines 19-31). Aydemir further discloses that switch 10 receives the pause frame and pauses the sub-queue of output queue 16a which corresponds to the stream identifier (Aydemir – col. 7, lines 32-37). Aydemir at col. 8, lines 53-65 discloses that after switch 10 determines the particular sub-queue identified by the stream identifier, switch 10 pauses that particular output sub-queue for a predetermined duration.

Therefore, Aydemir does not disclose that one of the sub-queues (such as sub-queue 18a alleged to be equivalent to the claimed first logic component) generates a pause frame and transmits the pause frame via the port identified by the receive port information, as required by amended claim 1. In contrast, Aydemir discloses that switch 10' (alleged to be equivalent to the second logic component) generates the pause frame and transmits it to switch 10. In addition, neither switch 10' nor switch 10 of Aydemir transmits a pause frame via the port identified by the receive port information, as further required by amended claim 1.

For at least these reasons, Aydemir does not disclose or suggest each of the features of amended claim 1. Accordingly, withdrawal of the rejection and allowance of claim 1 are respectfully requested.

Claims 2-5 are dependent on claim 1 and are believed to be allowable for at least the reasons claim 1 is allowable. In addition, these claims recite additional features not disclosed or suggested by Aydemir.

For example, claim 3, as amended, recites that the transmitting the pause frame comprises transmitting the pause frame via the port identified by the receive port information and not transmitting the pause frame by the first logic component via other ports on the first logic component.

Since Aydemir, as discussed above, does not disclose that any of the output port sub-queues 18a (or switch 10) transmits a pause frame, Aydemir cannot further disclose that any of the output port sub-queues 18a (or switch 10) transmits the pause frame via the port identified by the receive port information and does not transmit the pause frame via other ports on switch 10, as required by amended claim 3.

For at least this additional reason, withdrawal of the rejection and allowance of claim 3 are respectfully requested.

Claim 5 recites discarding the receive port information associated with the data frame after transferring the frame forwarding information to an output queue, when the condition is not detected. The Office Action states that Aydemir discloses this feature and points to col. 7, lines 19-24 for support (Office Action – page 4). The applicants respectfully disagree.

Initially, as discussed above, Aydemir does not disclose that switch 10' stores receive port information. Therefore, Aydemir cannot further disclose discarding the receive port information after transferring the frame forwarding information to the output queue, when the condition is not detected, as required by claim 5. Further, Aydemir at col. 7, lines 19-24 discloses that switches 10 and 10' may carry out normal processing and congestion related processing that includes pausing processing by an output port queue 16a on switch 10. This portion of Aydemir does not disclose or suggest discarding receive port information associated with the data frame after transferring the frame forwarding information to an output queue, when a condition is not detected, as required by claim 5.

For at least this additional reason, withdrawal of the rejection and allowance of claim 5 are respectfully requested.

Claim 15, as amended, recite features similar to claims 1 and 3. For reasons similar to those discussed above with respect to claims 1 and 3, Aydemir does not disclose or suggest each of the features of claim 15. Accordingly, withdrawal of the rejection and allowance of claim 15 are respectfully requested.

Claim 6 has been rejected under 35 U.S.C. § 103 as being unpatentable over Aydemir in view of Rom et al. (U.S. Patent No. 6,252,849; hereinafter Rom). The rejection is respectfully traversed.

Claim 6 depends on claim 1 and is believed to be allowable for at least the reasons claim 1 is allowable. Rom does not remedy the deficiencies discussed above with respect to claim 1. Accordingly, withdrawal of the rejection and allowance of claim 6 are respectfully requested.

Claim 18 was indicated as being allowable if rewritten in independent form. Claim 18 has hereby been rewritten in independent form to include the features of claim 15. Accordingly, allowance of claim 18 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____
Glenn Snyder
Reg. No. 41,428

Date: April 13, 2005

11240 Waples Mill Road
Suite 300
Fairfax, VA 22030
Telephone: (571) 432-0800
Facsimile: (571) 432-0808